REMARKS

The Office Action of February 1, 2006 has been carefully studied.

The substitute specification filed November 14, 2005 does not contain new matter.

Claims 5 and 7 have been canceled and rewritten as claims 28 and 29, respectively, and new claim 30, that depends on claim 29, has been added. Rewritten claim 29 does not include the alleged vague and indefinite aspect of claim 7. Claims 9 and 25 have been amended to overcome the rejection thereof on 35 U.S.C. §112, paragraph 2.

Applicants traverse the rejection of claims 3 and 4 under 35 U.S.C. §112, second paragraph. Applicants have previously argued why claim 3 is not vague and indefinite under 35 U.S.C. §112, second paragraph. The office action fails to include a rebuttal to applicants' position with regard to the rejection of claim 3 under 35 U.S.C. §112, second paragraph, and does not include a citation as requested in the last response. Until the examiner provides adequate rationale to overcome the arguments previously presented by applicants with regard to claim 3, claim 3 will not be amended to obviate the rejection thereof under 35 U.S.C. §112, second paragraph.

Applicants traverse the rejection under 35 U.S.C. §103(a) of claims 1, 3-9, 11-17 and 22-27 as being unpatentable over Bui et al., U.S. Patent 6,201,752, in view of Wanlass, U.S. Patent 3,356,858. The Office Action incorrectly alleges capacitive element 807 or 808 of the delay circuit of Figure 8a of Bui et al. meets the claim 1 requirements for at least one switchable capacitor for (1) preventing the paths of first and second transistors from being on simultaneously during transitions between first and second levels of a voltage source (not stated to be transitions between one and off states of the first and second transistors, for clarity) and (2) arranged to have an initial finite capacitance value during an initial part of a transition between the first and second levels of the

voltage source and to be switched from the initial finite capacitance value to a substantially open circuit in response to the voltage across the at least one switchable capacitor changing during the transition from one side of a threshold voltage to a second side of the threshold voltage, wherein the threshold voltage is between the first and second levels. The only description of Figure 8a in the Bui et al. reference is in column 3, lines 25-33. Nowhere is capacitive element 807 or 808 indicated as being switchable and in particular it is not indicated as having an initial finite capacitance value during an initial part of a transition between the first and second levels of the voltage source and to be switched from the initial finite capacitance value to a substantially open circuit in response to the voltage across the at least one switchable capacitor changing during the transition from one side of a threshold voltage to second side of the threshold voltage, wherein the threshold voltage is between the first and second levels.

The statement in the last sentence of the paragraph of the top of page 5 of the Office Action that the structure of claim 1 is fully met is wrong. The Office Action has not demonstrated that capacitive element 807 or 808 of Bui et al. has a structure associated with a threshold voltage between first and second levels of a voltage source. The threshold voltage of an electronic device is not a functional characteristic. Instead, it is a structural characteristic, similar to a temperature coefficient.

The reliance on *In re Best*, 562 F.2d 1252, 1254, 195USPQ 430, 433 (CCPA 1977) and *In re Schreiber*, 128 F.3rd 1473, 1477, 44 USPQ2d 1429, 1431 (Federal Circuit 1997) is incorrect. In the present case, the claimed and prior art products are not identical or substantially identical in structure because the Bui et al. capacitive elements are not switchable capacitors having threshold voltages between first and second levels of an input voltage source, as required by the Best decision. In the Schreiber case, the embodiment depicted in Figure 1 of the application had the same general

shape as an embodiment of the reference relied on by the U.S. Patent and Trademark Office. There is no analogous situation in the present case because, inter alia, of the threshold requirement of applicants' claim 1.

Also, Applicants' connections of NFET and PFET capacitors 32 and 34 to PFET 48 and NFET 50, as specified in claims 14 and 27-30, are entirely different from Bui's connections of capacitive elements 807 and 808 to the input of inverter 809. In the Bui et al. circuit, the gate electrodes of capacitive elements 807 and 808 have a common connection to a single input of inverter 809. The source and drain electrodes of PFET capacitive element 807 are connected to a positive DC power supply terminal, while the source and drain electrodes of NFET capacitive element 808 are grounded. In applicants' circuit, NFET 52 and PFET 54 are separately connected to PFET 48 and NFET 50 such that NFET 52 does not affect the current flowing to the gate electrode of NFET 50 and PFET 54 does not affect the current flowing to the gate electrode of PFET 48. In addition, the source and drain electrodes of NFET 52 are grounded, while the source and drain electrodes of PFET 54 are connected to a positive power supply voltage. Because of these differences between Applicants' circuit and the Bui et al. circuit, *In re Best* and *In re Schreiber* are not germane.

The text book CMOS Digital Integrated Circuits Analysis and Design, Kang et al, indicates the combination of Bui et al. and Wanlass, as proposed by the Examiner, would not include the requirement of the independent claims for circuitry including at least one voltage responsive switchable capacitor for preventing the paths of the first and second transistors from being on simultaneously during transitions between the first and second and levels, even if the Bui et al. capacitors were switchable. In the Bui et al. circuit, PFET 802 and NFET 806 are respectively off and on in response to the voltage on lead 801 being high; while the voltage on lead 801 is low,

PFET 802 is on and NFET 806 is off. While PFET 802 is on, current flows from the positive power supply terminal through the source drain path of PFET 802 and resistor 803, thence through capacitive element 808, causing the voltage at lead 804 and at the input of inverter 809 to increase in a generally exponential manner. While NFET 806 is on, current flows from the positive power supply terminal through capacitive element 807 and resistor 805, thence through the source drain path of NFET 806 to ground. The current flow through capacitive element 807 causes the voltage at lead 804 to decrease in a generally exponential manner. Hence, the voltage on lead 804, at the input of inverter 809, oscillates back and forth between two voltages, neither of which is at ground or the positive power supply voltage of the circuit. The generally exponentially oscillating voltage on lead 804 can not reach ground or the power supply voltage because the length of the pulses applied to lead 801 would be such as to prevent such operation. It is well recognized that unstable oscillator operations occur if an exponential wave is allowed to approach its maximum level. The voltage variations across capacitors 807 and 808 that result in the oscillations on lead 804 are preferably in the substantially linear initial portions of the exponential waves, i.e., far from the power supply voltages at the ends of the exponential waves. Hence, any switching characteristics of capacitors 807 and 808 would not influence the oscillating variations on lead 804.

In response to the oscillating variations on lead 804, NFET 10 and PFET 30 of Wanlass would be on simultaneously when the threshold of the Wanlass inverter circuitry is reached. In this regard, pages 172-190, Chapter 6 and a portion of Chapter 12 (all of which are enclosed as Applicants' Exhibit 1) indicate that inverters of the type disclosed by Wanlass have a short circuit current simultaneously flowing through both the NFET and the PFET of the inverters in response to the NFET and PFET transitioning between the on and off states thereof. Figure 5.17, on page 175, and the description thereof indicate that in the Wanlass inverter configuration (see Figure 5.16 on

page 173 of Kang et al.) both the pMOS and nMOS are insaturation for a considerable range of input voltages at the common gates of the NFET and PFET. Kang et al. discusses this situation, for example, on page 189 in the section entitled "Power and Area Considerations", where it is stated:

> In many applications requiring a low overall power consumption, CMOS is preferred over other circuit alternatives for this reason. It must be noted, however, that the CMOS inverter does conduct a significant amount of current during a *switching event*, i.e., when the output voltage changes from a low state to a high state, or from a high to low state.

The power dissipation occurring as a result of switching in such CMOS type inverters is also discussed in detail in section 6.7, pages 243-245 of Kang et al., and on pages 456-460 of Kang et al. The first two sentences of the second full paragraph on page 245 state:

> Note that under realistic conditions, when the input voltage waveform deviates from ideal step input and has nonzero rise and fall times, for example, both the nMOS and the pMOS transistor will simultaneously conduct a certain amount of current during the switching event. This is called the short-circuit current, since in this case, the two transistors temporarily form a conducting path between V_{DD} and the ground.

The foregoing discussion concerning inverters of the type disclosed by Wanlass also indicates that even if capacitive elements 807 and 808 were switched as recited in the independent claims, current would simultaneously flow through NFET 10 and NFET 30 of Wanlass during transitions of transistors 10 and 30 between the on and off states thereof. The previously discussed portions of Kang et al. clearly indicate the Wanlass inverter circuitry of Figure 5 is such that current simultaneously flows through NFET 10 and PFET 30 during switching of the inverter.

The allegation in the first full paragraph on page 8 of the Office Action that the operation of Figure 8A of Bui et al. meets all the method steps recited in claims 22-24 merely because the figure includes a circuit having first and second opposite conductivity transistors, opposite first and second

power supply terminals, an output terminal and first and second switchable capacitors is wrong. The examiner has not attempted to establish a prima facie case that the steps of claim 22, upon which claims 23 and 24 depend, are disclosed by his modification of Bui et al. as result of Wanlass. There is nothing in Bui et al. to indicate the first and second capacitors are switched off during the first and second intervals of claim 22.

With further regard to claim 22, the Eaminer has failed to indicate why Bui et al. causes the path of a first transistor in the Wanlass inverter to be turned off while maintaining the path of the second transistor in the Wanlass inverter off by changing a first voltage from a first value toward a second value while the first capacitor remains turned off. He has also failed to explain why Bui et al. causes the path of the second transistor in the Wanlass inverter to be turned off during an initial portion of a second transition period while maintaining the path of the first transistor in the Wanlass inverter off by changing the second voltage from the second value toward the first value while the second capacitor remains turned off. The Examiner has also failed to explain how Bui et al. includes the requirements of claim 23 to (1) switch off the first capacitor during the second portion of the first transitional period prior to the value of the first voltage, as applied to the control electrode of the first transistor in the inverter, reaching the first value, and (2) switch off the second capacitor during the second portion of the second transitional period prior to the value of the second voltage, as applied to the control electrode of the first transistor in the inverter, reaching the second value.

The foregoing analysis of the Examiner's proposed combination of Bui et al. and Wanlass also demonstrates that the requirement of method claim 22 for turning off the path of a first transistor while maintaining the path of a second transistor off during an initial portion of a first transitional period between on and off intervals of the first and second transistors by changing the

first voltage from the first value toward the second value while the first capacitor remains turned off and the second capacitor is charged is not found in the combination. In addition, the foregoing analysis indicates that the requirement of claim 22 for turning off the path of the second transistor while maintaining the path of the first transistor off during an initial portion of a second transitional period between first and second intervals by changing the second voltage from the second value toward the first value while the second capacitor remains turned off and the first capacitor is charged is not found in the proposed combination. These steps can not occur in the proposed combination because the Kang et al. citation indicates the short circuit current simultaneously flows in NFET 10 and PFET 30 of Wanlass during a transition.

The foregoing analysis also indicates that the proposed combination of Bui et al. and Wanlass fails to include the requirement of claim 26 for a first transistor to be turned off and remain turned off until after a second transition between the levels of a bi-level signal occurs, wherein the second transition is in a direction opposite from a first transition, and the requirement for the second transistor to be initially off. Similarly, in response to the second transition, the second transistor is required by the claim to be turned off and remain turned off until after the first transition and the first transistor is initially off. Hence, claim 26 requires the first and second transistors to be simultaneously off during the first and second transitions.

In the rejection of claims 26 and 27, the Examiner comments that, because every transistor must have a threshold voltage, NMOS 808 and PMOS 807 have third and fourth thresholds. However, this comment ignores the structural requirement of claim 26, upon which claim 27 depends, for the third and fourth thresholds to between the voltages at the first and second power supply terminals for causing the capacitors to have finite values and be switched off in response to the voltages across the capacitors being on opposite sides of the thresholds. The Examiner has also

ignored requirements (I) and (II) of claim 26. *In re Best* and *In re Schreiber* are no more applicable to requirements (I) and (II) of claim 26 than they are to claim 1 for the reasons discussed supra.

The foregoing analysis clearly indicates the proposed combination of Bui et al. and Wanlass does not meet the terms of the independent claims.

The claims dependent on claim 1 are allowable for the same reasons advanced for claim 1. In addition, the comments on page 6 of the Office Action concerning claims 8, 9 and 25 ignore the fact that Bui et al. fails to disclose first and second switchable capacitors. Bui et al. also fails to disclose the structural requirement of claim 9 that the first capacitor has a finite capacitance value on a first side of a first threshold and a substantially open circuit on a second side of the first threshold and a second capacitor that has a finite capacitance value on a second side of a second voltage threshold and an open circuit on a first side of the second threshold, wherein the first and second thresholds differ from each other and are between the first and second levels. As pointed out supra, a threshold of an electronic component is a structural attribute, not a functional result. A threshold of an electronic component is similar to a temperature coefficient, which certainly cannot be considered a functional result. While the threshold of a PMOS transistor may differ from the threshold of an NMOS transistor, there is nothing to indicate the Bui et al. capacitive elements 807 and 808 have thresholds between the first and second levels as set forth in claim 1, on which claims 9 and 25 depend.

Claim 27, that depends on claim 26, is amended to further distinguish over the applied references by requiring the N doped FET capacitor device to be connected so that it does not affect current flowing to the gate electrode of the NFET second transistor and the P doped FET capacitor device to be connected so that it does not affect current flowing to the gate electrode of the PFET first transistor.

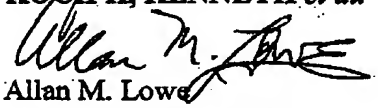
New claims 28-30 include limitations somewhat similar to the foregoing limitation of claim 27. The oscillating wave resulting from the current flowing through capacitive elements 807 and 808 of Bui et al. affect the operation of both transistors in inverter 809 because the capacitive elements are connected to a single common input terminal of the inverter.

In view the foregoing amendments and remarks, favorable reconsideration and allowance are respectfully requested and deemed in order.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 08-2025, and please credit any excess fees to such deposit account.

Respectfully submitted,

KOCH II, KENNETH *et al.*



Allan M. Lowe
Registration No. 19,641

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400
Telephone: 703-684-1111
Facsimile: 970-898-0640

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